ABSTRACT

A fabrication process for a silicon-on-insulator (SOI) device includes defining an active region in an SOI substrate, doping the entire active region with an impurity of a given conductive type, masking a main part of the active region, and doping the peripheral parts of the active region at least two additional times with an impurity of the same conductive type, preferably using different doping parameters each time. The additional doping creates a channel stop in the peripheral parts of the active region, counteracting the tendency of the transistor threshold voltage to be lowered in the peripheral parts of the active region, thereby mitigating or eliminating the unwanted subthreshold hump often found in the transistor operating characteristics of, for example, fully depleted SOI devices.